Workshop on Advanced Computer Architectures and Dependable Embedded Systems
by Tallinn University of Technology

Background: Innovative chip manufacturing technologies are the key enabling factors for modern IT systems. Driven by Moore’s Law, the functional integration density on microchips permanently increasing. This enables hardware and system designers to successfully realize advanced System-on-Chip solutions for embedded computing (mobile phones, computing pads, photo cameras, medical devices, automotive electronics, avionic systems, infotainment products), which have strict demands for low power consumption at increasing functional complexity. In the field of high-performance computing similar requirements are becoming more and more important: scalable multiprocessor computing systems on different integration levels: MultiProcessor System-on-Chip (MPSOC), servers, data centers, private and public clouds.

Gain and content: In this workshop the participants will learn about systematic and CAD supported structuring of hardware and computer architectures. First we derive some basic methods for architectural synthesis. Then we will step up several layers of abstraction and analyze, how this methods can be used for the design of complex on-chip multiprocessor architectures. In this context advanced on-chip communication architectures are an integral part of this course.

The workshop will be held during 2 days with 6 academic hours every day (can be changed). The workshop consists of two parts (one for each day):
1. Introduction to CAD methods for Hardware and System Architecture Synthesis:
   a. Introduction to CAD methods for chip and system design
   b. Synthesis of processing architectures out of sequential program code (Architectural Synthesis
   c. Efficient resource usage by application of scheduling methods
2. Advanced On-Chip Multiprocessor Architectures with Network-on-Chip Communication
   a. Networks-on-Chip as efficient on-chip communication architectures: topologies, switching and routing methods
   b. Multiprocessor Systems-on-Chip (MPSoC) based on 3D chip stacking
   c. Virtualisation and Dependability/Reliability concepts for MPSoCs

Participants / Target group:
Students at the end of the Bachelor level or in master studies in the fields of Computer Engineering, Electronics Engineering, Mechatronics, Computer Science. Students should have a good knowledge on logic circuit design and logic optimization and computer architectures (controllers, datapathes). Furthermore some know-how on hardware modeling and sequential an object-oriented programming will be helpful as well as some basic know-how on optimization methods and complexity theory.

Instructor: Thomas Hollstein is Professor in the Department of Computer Engineering at Tallinn University of Technology (TTU). He graduated from Darmstadt University of Technology in Electrical Engineering / Computer Engineering in 1991. In 2000 he received his Ph.D. on “Design and interactive Hardware/Software Partitioning of complex heterogeneous Systems” at Darmstadt University of Technology. He has an extensive industrial background in the field of embedded HW/SW systems and printable electronics. Since September 2010 Thomas Hollstein is a full professor at TTU leading the research team "Dependable Embedded Systems". His research interests are in the fields Dependable Embedded Systems, System-on-Chip Design, Networks-on-Chip, MPSoCs (Programming Models, APIs), Reconfigurable Systems and Printed Electronics. Thomas Hollstein has published over 60 peer-reviewed papers and is member of the programme committees of several international conferences and workshops.

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