Approximate Computing in Wireless Heart-Rate Monitoring: Design and Implementation on FPGA

Context
(Similar to the one in my other MSc thesis proposal "Compressive Sensing for Wireless Heart-Rate Monitoring: Design and Implementation on FPGA")

Heart Rate Monitoring (HRM) is available in an increasing number of applications, including health and fitness, professional training, and condition and health monitoring. In many cases it is desirable that the link between the sensing node and computing node (e.g. mobile phone) be wireless for the convenience of the users. However, transmitting data wirelessly over a radio link is an energy-consuming process that can significantly reduce the battery life-time of the sensing nodes. Furthermore, in many applications it is preferable, or even necessary, to rely on low-rate technologies such as 6LoWPAN.

Given the above, it is thus desirable to reduce the amount of data to be transmitted. While compressed sensing (CS) has recently emerged as an attractive solution to this problem, another recent trend has started to be applied in wireless HRM, namely approximate computing, also known as inexact computing.

Objective
The main objective of this MSc thesis is to design, simulate, and possibly implement one or several approximate computing techniques in a wireless HRM targeting a low-power platform such as Microsemi’s IGLOO nano low-power FPGA [1]. The pre-identified techniques are described in [2], [3], and [4], but other techniques can be selected by the student(s). Moreover, it is proposed to consider the work conducted together in cooperation with Aalborg University [5] as a possible base and/or reference system.

Possible tasks
- Get an understanding of the work presented in [2], [3], [4], and [5].
- Survey the literature for other architectures and implementations
- Get an understanding of Microsemi’s IGLOO nano low-power FPGA architecture and corresponding tool ('Libero SoC').
- Design, simulate, and synthesize one or several approximate computing technique(s).
- Analyze the results and possibly optimize the design.
- Pending availability, test on real hardware.

References

[5] M. El-Sayed and S. Lund, ”An FPGA-friendly Compressed Sampling Engine for WSN-based Heart Rate Monitoring”, Project report, Aalborg University, Denmark, 2015 (provided on request, see below)

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