Nano- and Micro-scale Simulations of Ge/3C-SiC and Ge/4H-SiC NN-heterojunction Diodes

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Abstract. During the last decade, silicon carbide (SiC) and its heterostructures with other semiconductors have gained a significance importance for wide range of electronics applications. These structures are highly suitable for high frequency and high power applications in extremely high temperature environments. SiC exists in more than 200 different polycrystalline forms, called polytypes. Among these 200 types, the most prominent polytypes with exceptional physical and electrical attributes are 3C-SiC, 4H-SiC and 6H-SiC. Heterostructures of these SiC polytypes with other conventional semiconductors (like Si, Ge) can give rise to interesting electronic characteristics. In this article, Germanium (Ge) has been used to make heterostructures with 3C-SiC and 4H-SiC using a novel technique called diffusion welding. Microscale and nanoscale simulations of nn-heterojunction of Ge/3C-SiC and Ge/4H-SiC have been done. Microscale devices have been simulated with a commercially available semiconductor device simulator tool called Silvaco TCAD. Whereas nanoscale devices have been simulated with QuantumWise Atomistix Toolkit (ATK) software package. Current-voltage (IV) curves of all simulated devices have been calculated and compared. In nanoscale device, the effects of defects on IV-characteristics due to non-ideal bonding (lattice misplacement) at heterojunction interface have been analyzed. Our simulation results reveal that the proposed heterostructure devices with diffusion welding of wafers are theoretically possible. These simulations are the preparations of our near future physical experiments targeted to fabricate high electron mobility power diodes or LEDs by diffusion bonding of the wafers.

Introduction

Semiconductor heterostructures are the most essential component of the modern solid-state devices. Heterostructures are being used widely in almost every electronic device like light-emitting diodes (LEDs), bipolar junction transistors, and telecommunication applications [1]. The motion of the charge carriers and states can be precisely controlled in the heterostructure devices at design stage by choosing appropriate semiconductor materials. Heterostructure device performance can be improved due to the control on energy band profile during the design phase [2]. In recent years, Silicon carbide (a wide bandgap semiconductor material) has gained significant importance for the fabrication of heterostructures devices. SiC exists in several crystalline forms called polytypes. Each polype exhibits unique electrical and physical properties [3]. The wide bandgap of SiC significantly reduces the generation of electron-hole pairs caused by thermal activation. Therefore, SiC has high thermal conductivity and chemical tolerance. That is why SiC based electronic devices are highly suitable for high temperature electronic applications [4].
Figure 1. (a) Geometry of the Ge/3C-SiC nanoscale simulated device; (b) Ge/4H-SiC nanoscale device without axial defects; (c) Ge/4H-SiC nanoscale
device with axial interface defects; (d) Geometry of microscale simulated device; (e) Side-view of quasi 2D nanoscale simulated devices

Figure 2. (a) Forward and (b) reverse IV-characteristics of microscale and nanoscale Ge/3C-SiC devices [For actual current values read *current axis in Ampere; **current axis in nano-Ampere]

Moreover, germanium (Ge) is also a popular semiconductor that has been also widely used for the electronic applications. Heterostructures based on SiC and Ge may give rise to interesting electronic properties in the resultant devices. So far the epitaxial growth technology has been considered as the most well studied technology for the fabrication of SiC based devices with predictable results [5]. Some other the state of the art techniques to fabricate heterostructures of SiC with stable yield and promising results are chemical vapour deposition (CVD), liquid-phase epitaxy (LPE) and molecular beam epitaxy (MBE). In these techniques, a thin epitaxial layer of one type of semiconductor material is deposited on the other thick wafer/substrate [6].

In this article, we proposed/used a novel technique (diffusion bonding) to fabricate SiC and Ge heterostructures by direct bonding of their wafers. This technique has rarely been used for joining two semiconductor wafers. The principle of diffusion bonding/welding is solid state diffusion. This techniques is usually used to join dissimilar metals with each other. But our proposal is to use it for joining SiC with Ge wafers directly to make heterostructure diodes like Ge/3C-SiC and Ge/4H-SiC. In this article micro and nanoscale simulations have been done for Ge/3C-SiC and Ge/4H-SiC. The fabrication of our proposed devices with diffusion bonding will reduce the fabrication efforts and improve the device performance [7].

Figure 3. (a) Forward IV-characteristics of microscale and nanoscale Ge/4H-SiC devices [To get actual current units *current axis x10⁻¹ Ampere; **current axis in nano-Ampere; ***current axis in nano-Ampere ;(b) reverse IV-characteristics of microscale and nanoscale Ge/4H-SiC devices [To get actual current units *current axis x10⁻¹⁵ Ampere; **current axis in nano-Ampere; ***current axis in nano-Ampere]
Methodology

The proposed devices (Ge/3C-SiC and Ge/4H-SiC) have been simulated both at microscale and nanoscale levels. For microscale simulations, a commercially available software Silvaco TCAD has been used. It includes several material related parameters and in-built physical models to simulate semiconductor devices. The geometry of microscale simulated device is shown in Fig.1(d). A 300µm thick wafer of Ge has been bonded with 4H-SiC and 3C-SiC wafer of same thickness in two different experiments by considering diffusion bonding technique. Ohmic contacts have been introduced at the top and bottom of this structure. Cross sectional area of each microscale device is 1x1 µm². Donor doping concentration for Ge, 3C-SiC and 4H-SiC has been chosen as 10¹⁸ cm⁻³. Finally IV-characteristics of the simulated devices (Ge/3C-SiC and Ge/4H-SiC) have been obtained using Tonyplot Command of Silvaco TCAD.

Furthermore, the nanoscale simulations have been performed within a high power computing environment (hpc) [8]. Each IV-curve took around more than two weeks to calculate in this hpc environment. The nanoscale simulations have been done with a nanoscale semiconductor device simulator, QuantumWise Atomistix Toolkit (ATK). ATK has in-built user interface tool which is called Virtual Nanolab (VNL). ATK together with this Virtual Nanolab tool is called ATK-VNL. ATK uses numerous in-built models to calculate the electronic properties of quantum systems. In these simulations, density functional theory (DFT) model of ATK has been used to calculate the electronic properties of the simulated devices. Mathematical model used by ATK-DFT calculator has been given in [9]. The nanoscale simulated devices has been shown in Fig.1(a),(b), (c). Each device is a quasi 2D structure with left and right electrodes (each electrode is 1 nm long). The central region of the device is 5nm long as shown in Fig.1(a). The side view of nanoscale device has been shown in Fig.1(e). The dimensions of the device in this Fig.1(e) are in the range of angstrom (Å). Donor doping concentration for Ge, 3C-SiC and 4H-SiC has been chosen as 10¹⁸ cm⁻³ to guarantee low breakdown voltage in the reverse-biased condition. For Ge/3C-SiC based nn-heterojunction device, Ge is (001)-oriented and 3C-SiC is (111)-oriented. Whereas for Ge/4H-SiC based nn-heterojunction device, Ge is (001)-oriented and 4H-SiC is (0001)-oriented. Ge/3C-SiC and Ge/4H-SiC heterostructures have been simulated in above mentioned orientations. Semiconductors themselves have been chosen as electrodes to avoid Schottky contact formation at contacts.

Moreover, lattice misplacement defects due to non-ideal bonding of wafer have been intentionally introduced at the heterojunction interface of Ge/4H-SiC based device. (001)-oriented Ge and (0001)-oriented 4H-SiC have been twisted at an angle of 12 degrees with respect to each other to produce lattice misplacement defects, as shown in Fig.1(c). Finally, IV-characteristics of all nanoscale simulate devices have been calculated and analyzed.

Results and Discussion

The micro- and nanoscale simulation results have been shown in Fig. 2 and Fig. 3. The forward characteristics of micro- and nanoscale Ge/3C-SiC devices have been shown in Fig.2(a). The simulation results in forward biased condition are similar to a conventional pn-junction diode. Microscale Ge/3C-SiC device starts to conduct electric current at relatively very low bias voltage (around 0.1 V). Whereas the nanoscale device turns on at approximately 0.4 V. The difference in electron affinities dictates the barrier height at the heterojunction interface of two different semiconductors [10]. The conduction band offset at Ge/3C-SiC nn-heterojunction interface is 0.17 eV, calculated with electron affinity rule. This barrier height is quite low due to which the Ge/3C-SiC device starts to conduct at very low forward biased voltage, as shown in Fig.2(a). The reverse breakdown in microscale Ge/3C-SiC device also occurs at a very low negative bias voltage. It almost shows resistive behavior in both forward and reverse bias regime, as shown in Fig.2(a),(b). The possible reason of this behavior could be a small difference in electron affinities of Ge and 3C-SiC, which dictates the barrier height at heterojunction interface of Ge/3C-SiC based device, as shown in Fig.2 (b). The reverse breakdown in microscale device Ge/3C-SiC device occurs immediately after apply reverse voltage and device starts to conduct electric current, as shown in curve-1 of Fig.2(b). In nanoscale Ge/3C-SiC device, the reverse break down also occurs at
very low reverse voltage of approximately -0.4 V, as shown in curve-2 of Fig.2(b). The possible reason of this low reverse breakdown voltage could be the low value of barrier height at heterojunction interface due to small difference in electron affinities of Ge and 3C-SiC.

Furthermore, micro- and nanoscale simulation results for Ge/4H-SiC nn-heterojunction devices have been shown in Fig.3. Nanoscale Ge/4H-SiC has been simulated without lattice mismatch defects and also with lattice mismatch defects. These defects have been introduced intentionally at the heterojunction interface of Ge/4H-SiC based device to analyze the effects of non-ideal bonding on the IV-characteristics, as shown in Fig.1(c). The forward characteristics of Ge/4H-SiC based devices have been shown in Fig.3(a). The nanoscale device with and without defects turn on at almost the same forward bias voltage, as shown in Fig.3(a) [see curve2 and curve3]. They start to conduct electric current at approximately 0.3 V. But a decrease in current through the defective nanoscale device can be observed in Fig. 3(a) [see curve3] compared to that of without defects. Axial defects in nanoscale Ge/4H-SiC defective device probably provoke scattering phenomenon. This scattering contributes to reduce the forward current in defective device. The inclusion of lattice mismatch defects in nanoscale device actually influence the current through the device by stimulating electron and phonon scattering in the device. Moreover, these simulations have been done at 300 K. At this low temperature, electrons have less thermal velocity. These electrons with less thermal velocity are strongly influenced by the ionized impurities that deflect their path due to Coulombic forces. The wave function of electrons is also changed due to defects and scattering of charge carriers [11].

Moreover, the reverse IV-characteristics of micro- and nanoscale Ge/4H-SiC based nn-heterojunction devices have been calculated. The microscale simulated device starts to conduct electric current at a very low reverse bias voltage (at -1 V). The initial reverse current probably flows due to Zener effect which appears at approximately -1 V, as shown in curve-1 of Fig.3(b). The device becomes fully conductive in reverse bias regime at approximately -15 V due to avalanche breakdown, as shown in Fig.3(b). It has been observed that the reverse breakdown in the nanoscale Ge/4H-SiC device without defects occurs at approximately -0.7V. The same nanoscale device with axial defects at heterojunction interface starts to conduct reverse current at relatively high reverse voltage of about -1 V compared to that of without defects. The possible reason of this reverse breakdown at relatively high voltages in Ge/4H-SiC based devices could be high value of conduction band-offset compared to that of Ge/3C-SiC. For the Ge/4H-SiC based devices, the value of band-offset is 0.76 eV (according to electron affinity rule). An increase in reverse breakdown voltage has been observed in defective Ge/4H-SiV based nanoscale device, as shown in curve-3 of Fig.3(b). One of the main reasons of this increase could be the increase in scattering phenomenon which is enhanced by lattice mismatch defects at the heterojunction interface of this device [12].

Summary

Our simulation results revealed that the characteristics of Ge/3C-SiC and Ge/4H-SiC in forward bias regime are quite similar to the typical pn-junction diodes. Whereas reverse IV-characteristics of these device are significantly different from pn-junction diodes. These deviations from the ordinary behavior of pn-junction devices could be minimized by parameter tuning of the impact ionization and tunneling models in microscale devices. Whereas in nanoscale devices, such differences can be minimized by proper sizing of the devices. These results also disclosed that the inclusion of axial defects provoked the scattering process in the defective nanoscale devices. This increase in scattering of charge-carriers subsequently reduced the forward current and caused reverse break down to occur at relatively high voltages compared to that of the device without defects. These simulations show that theoretically it is possible to develop Ge, 3C-SiC and 4H-SiC based heterostructure devices with diffusion bonding. Our near future work includes the physical fabrication of the above mentioned simulated device with diffusion bonding technique to develop power diodes and LEDs.

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